LISTING OF CLAIMS

1-8. (Canceled)

9. **(Currently Amended)** A method for ~~testing~~ **measuring timing properties of at least one input/output circuit of** an integrated device comprising:

pulling in a strobe edge in predetermined decrements up to a single phase of a clock signal;

inverting the clock signal after the strobe edge has been pulled in by at least the single phase of the clock signal;

holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock signal, while pushing a data out in predetermined increments;

strobing **[[a]] the** data with **[[a]] the** strobe edge; **[[and]]**

measuring a setup parameter ~~for at least one~~ **of the** input/output circuit**; and** ~~by pulling in the strobe edge in predetermined decrements up to a single phase of a clock, inverting the clock after the strobe edge has been pulled in by at least the single phase of the clock; and holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock, while pushing the data out in predetermined increments.~~

determining whether a failure condition exists for the input/output circuit based on the measured setup parameter.

10. (Previously Presented) The method of claim 9 measuring the setup parameter comprises providing data from a functional logic block (FLB) within the integrated device.

11. (Original) The method of claim 10 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

12. **(Currently Amended)** The method of claim 9 wherein the strobe edge is on a falling edge of the clock **signal** and the data is on the rising edge of the clock **signal**.

13. (Original) The method of claim 9 wherein pushing the data comprises pushing out a rising edge of the inverted clock **signal**.

14. (**Currently Amended**) A method for ~~testing~~ **measuring timing properties of at least one input/output circuit of** an integrated device comprising:

pulling in a strobe edge in predetermined decrements up to a single phase of a clock signal;

inverting the clock signal after the strobe edge has been pulled in by at least the single phase of the clock signal;

holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock signal, while pushing data out in predetermined increments;

strobing **[[a]] the** data with **[[a]] the** strobe edge;

measuring a hold parameter ~~for at least one~~ **of the** input/output circuit**; and** ~~by pulling in the strobe edge in predetermined decrements up to a single phase of a clock, inverting the clock after the strobe edge has been pulled in by at least the single phase of the clock; and holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock, while pushing the data out in predetermined increments~~.

determining whether a failure condition exists for the input/output circuit based on the measured hold parameter.

15. (Previously Presented) The method of claim 14 measuring the hold parameter comprises providing data from a functional logic block (FLB) within the integrated device.

16. (Original) The method of claim 15 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

17. (**Currently Amended**) The method of claim 14 wherein the strobe edge is on a falling edge of the clock **signal** and the data is on the rising edge of the clock **signal**.

18. (**Currently Amended**) The method of claim 14 wherein pushing the data comprises pushing out a rising edge of the inverted clock **signal**.

19-24. (Cancelled)

25. (**Currently Amended**) An apparatus comprising:

a plurality of input/output ~~circuit~~ **circuits** to be tested by a central control loopback test that:

_____strobes a data with a strobe edge; and

_____measures a setup parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock **signal**;

the apparatus to invert the clock **signal** after the strobe edge has been pulled in by at least the single phase of the clock **signal**; and hold the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock **signal**, while pushing the data out in predetermined increments.

26. (Canceled)

27. (Previously Presented) The apparatus of claim 25 wherein the apparatus is a processor.